

Eight-block division power_supply scheme control signal generator for the subretinal prosthesis

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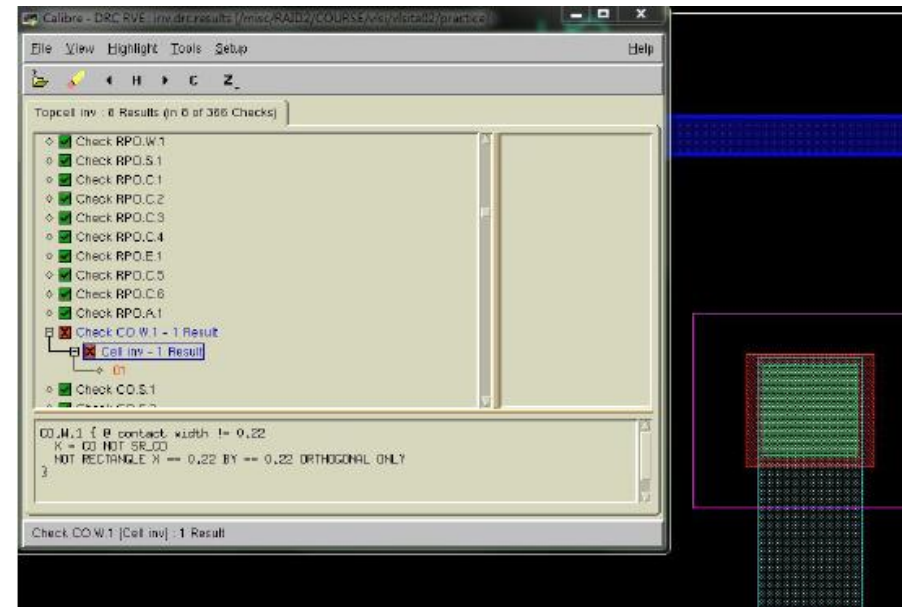
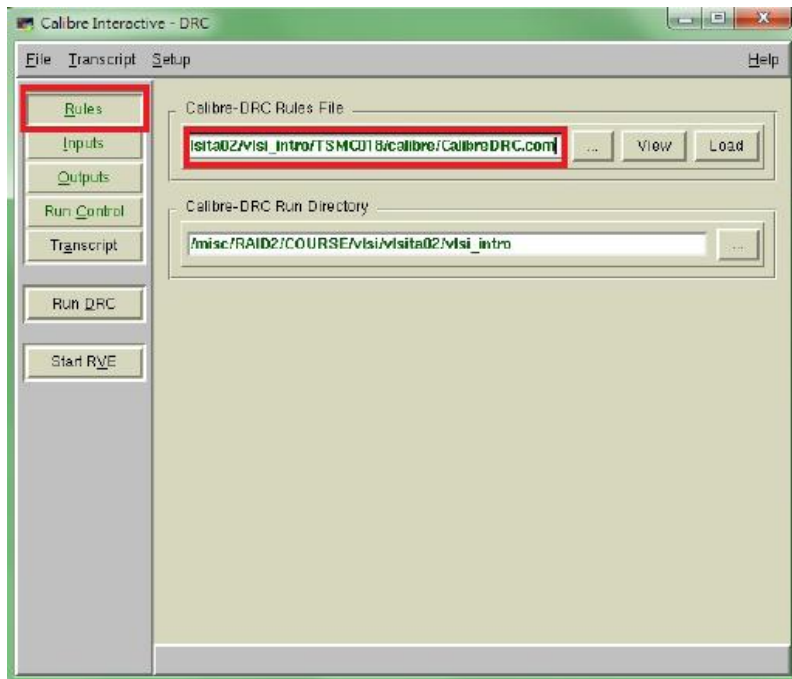
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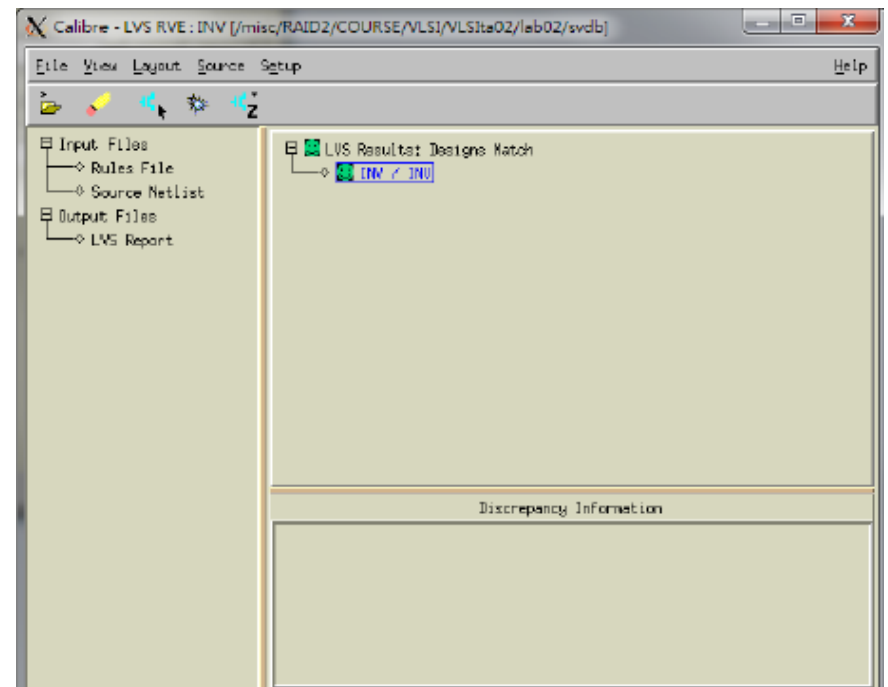
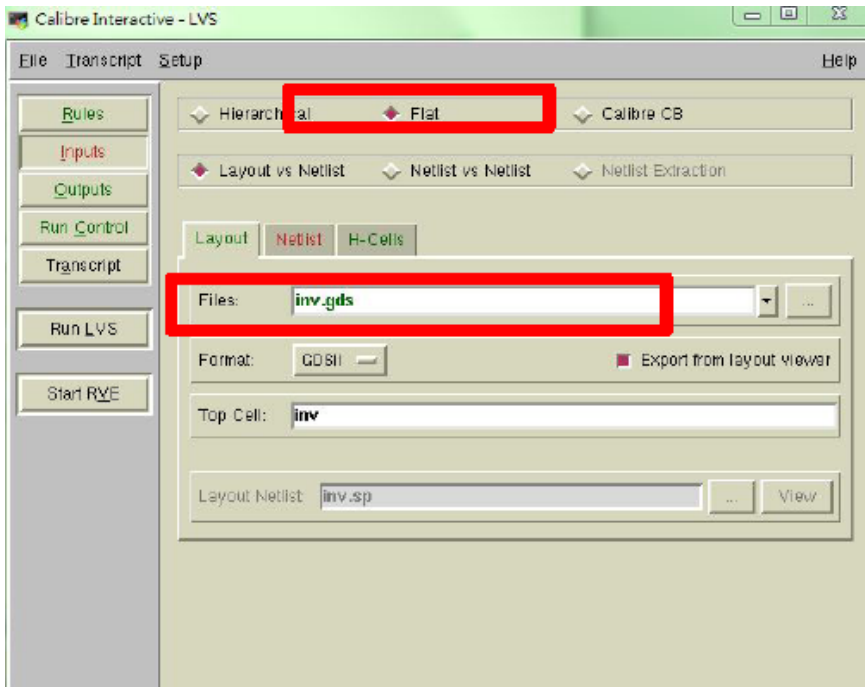
Layout Tool–Laker

- DRC(Design Rule Check)
- DRC is the area of Electronic Design Automation that determines whether the physical layout of a particular chip layout satisfies a series of recommended parameters called Design Rules.



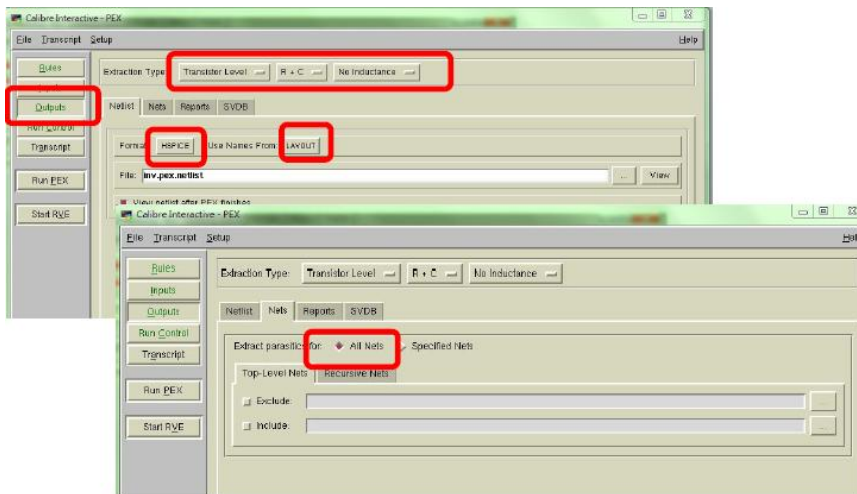
Layout Tool–Laker

- LVS(Layout Versus Schematic)
- LVS us the class of electronic design automation(EDA) verification software that determines whether a particular integrated circuit layout corresponds to the original schematic or circuit diagram of the design.



Layout Tool–Laker

- PEX(Parasitic Extraction)
- Parasitic Extraction is calculation of the parasitic effects in both the designed devices and the required wiring interconnects of an electronic circuit.

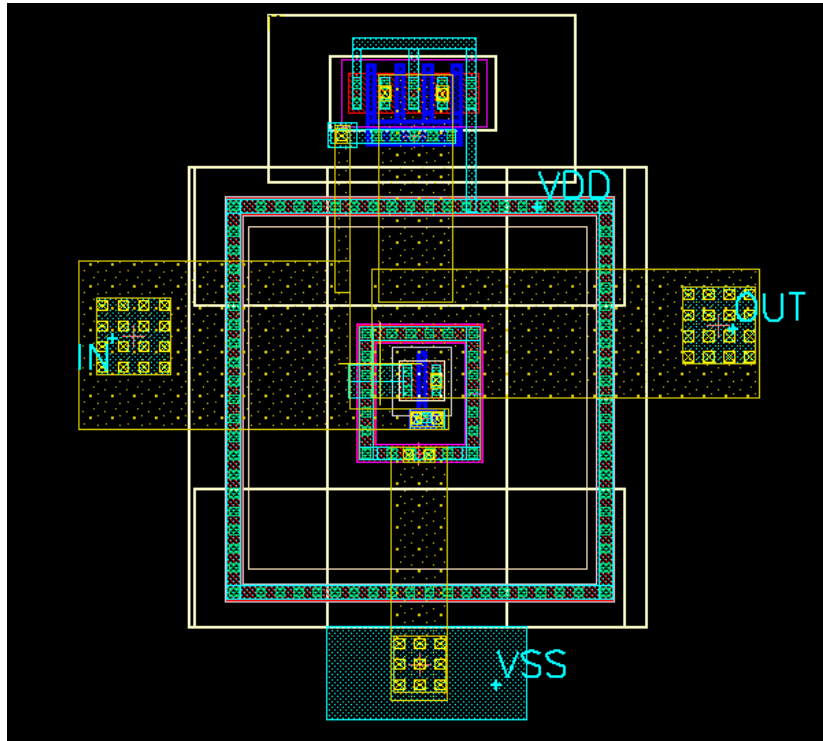


```
* File: inv.pex.netlist
* Created: Thu Nov 1 12:28:34 2012
* Program "Calibre XRC"
* Version "v2006.2_16.16"

.lib "mm018.l" TT

.include "inv.pex.netlist.pex"
.subckt INV GND VDD OUT IN
*
* IN IN
* OUT OUT
* VDD VDD
* GND GND
mM0 N_OUT_M0_d N_IN_M0_g N_GND_M0_s N_GND_M0_t inch=1.0e-07 W=1.125e-06
+ AD=6.4695e-13 AS=6.583e-13 PD=3.41e-06 PS=3.43e-06 NRD=0.502203 NRS=0.511013
mM1 N_OUT_M1_d N_IN_M1_g N_VDD_M1_s N_VDD_M1_t pch=1.8e-07 W=1.125e-06
+ AD=6.4695e-13 AS=6.583e-13 PD=3.41e-06 PS=3.43e-06 NRD=0.502203 NRS=0.511013
*
.include "inv.pex.netlist.INV.px1"
*
.ends
*
```

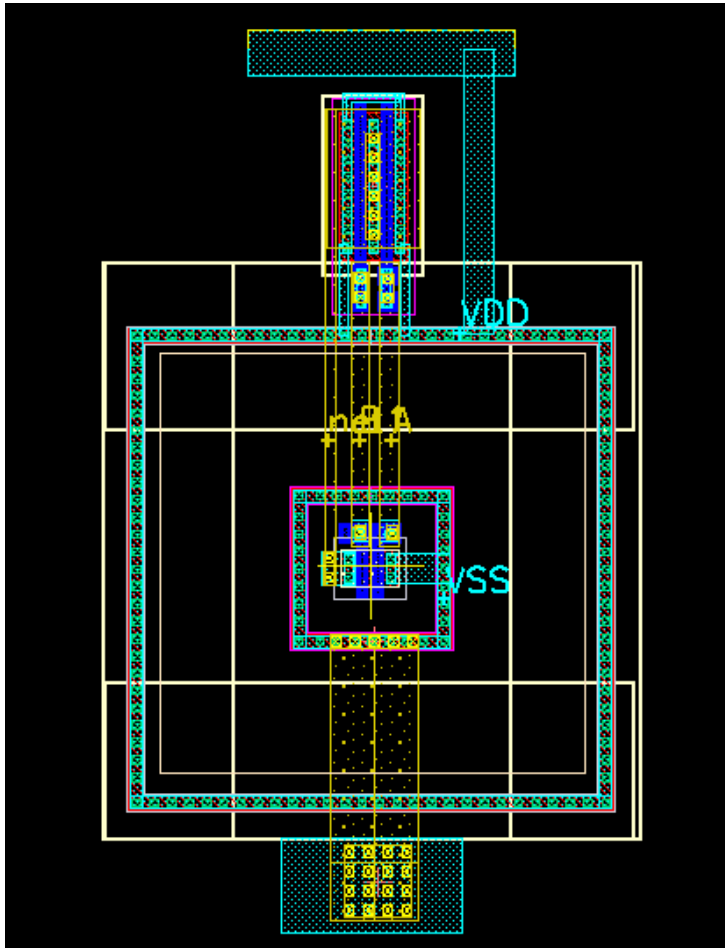
Layout Result – NVERTER



```
.SUBCKT INV IN OUT VDD VSS
xM1 OUT IN VSS VSS nch_mis W=.5u
L=.18u m=1
xM2 OUT IN VDD VDD pch_mis W=.5u
L=.18u m=4
.ends
```



Layout Result – NAND



```
.SUBCKT NAND A B net1 VDD VSS  
xM1 net1 A VDD VDD pch_mis W=1u  
L=.18u m=4  
xM2 net1 A net2 net2 nch_mis W=1u L=.18u  
m=1  
xM3 net2 B VSS VSS nch_mis W=1u L=.18u  
m=1  
xM4 net1 B VDD VDD pch_mis W=1u  
L=.18u m=4  
.ends
```