Eight-block division power_supply scheme control signal generator for the subretinal prosthesis

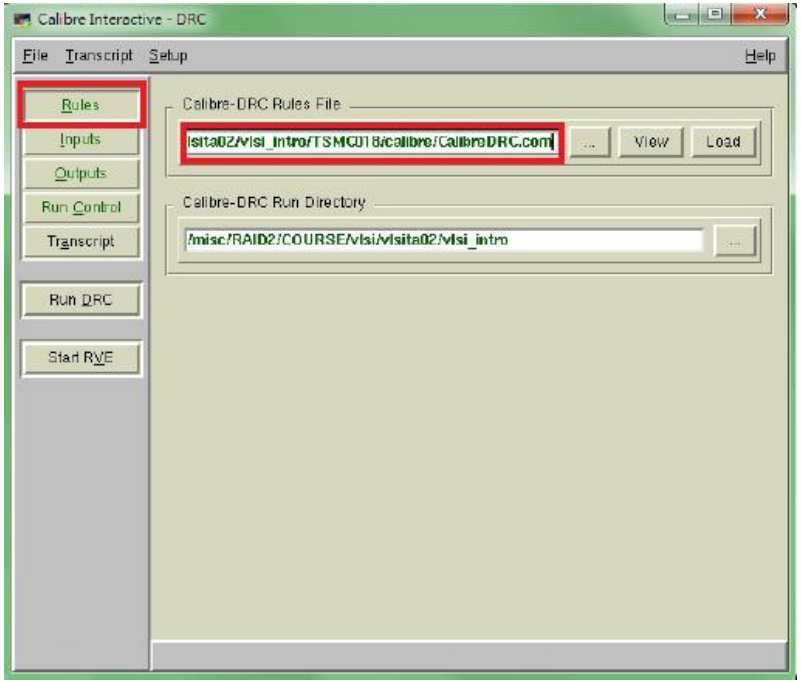
專 題 生：吳芮綺　　Jui-Chi Wu

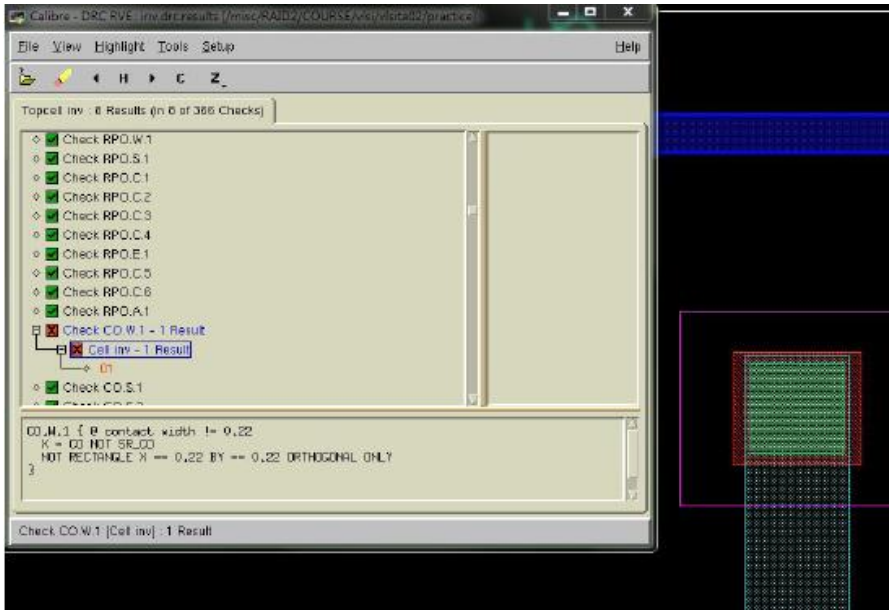
指導教授：吳重雨　　Chung-Yu Wu

Institute of Electronics and Department of Electronics Engineering
National Chiao Tung University
Hsinchu, TAIWAN

Layout Tool–Laker

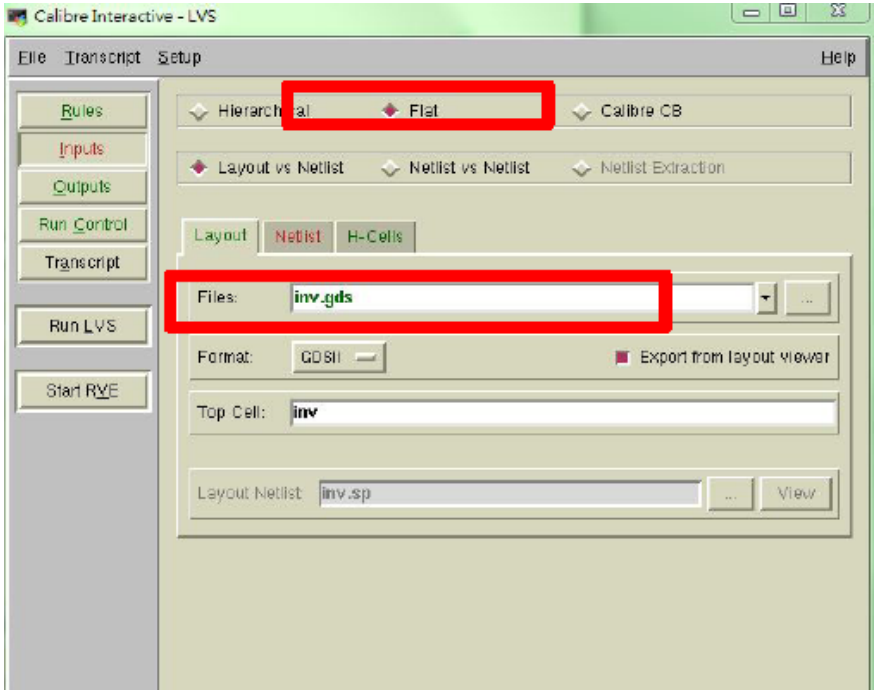
- DRC(Design Rule Check)
- DRC is the area of Electronic Design Automation that determines whether the physical layout of a particular chip layout satisfies a series of recommended parameters called Design Rules.

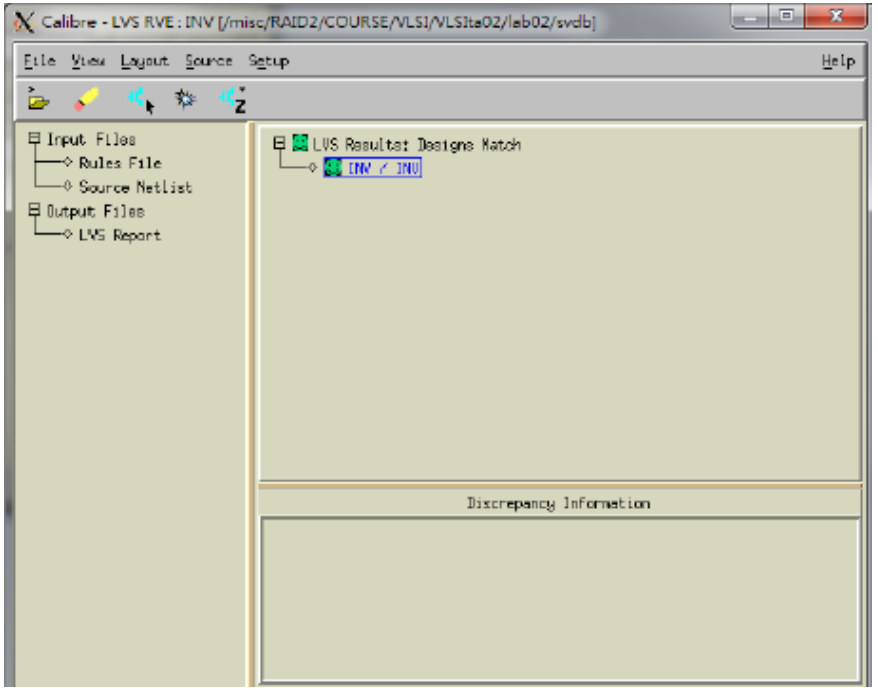




Layout Tool–Laker

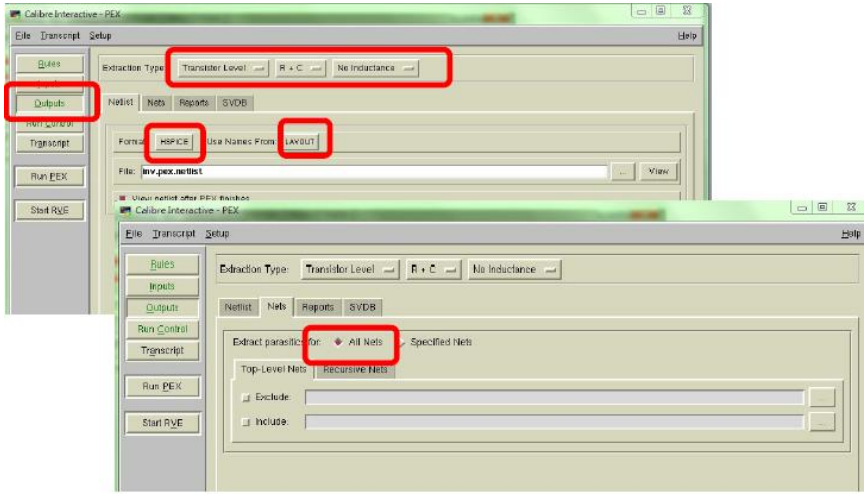
- LVS(Layout Versus Schematic)
- LVS us the class of electronic design automation(EDA) verification software that determines whether a particular integrated circuit layout corresponds to the original schematic or circuit diagram of the design.

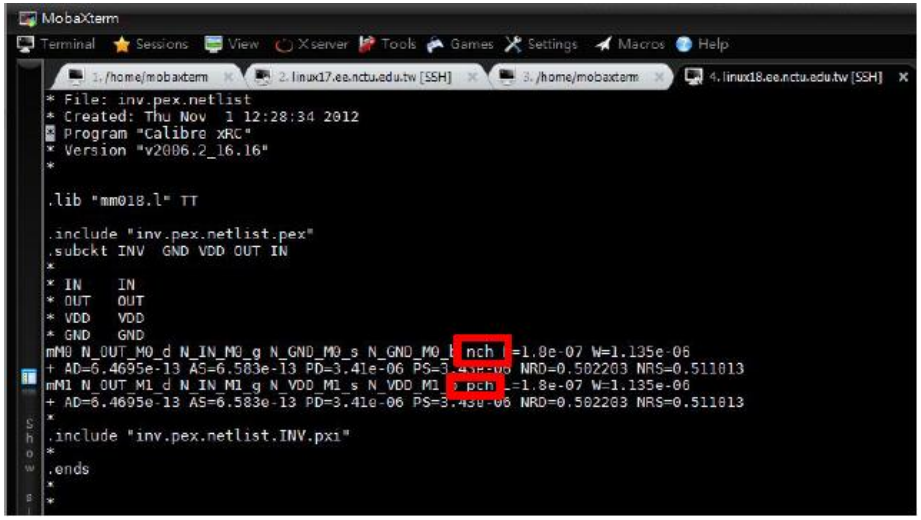




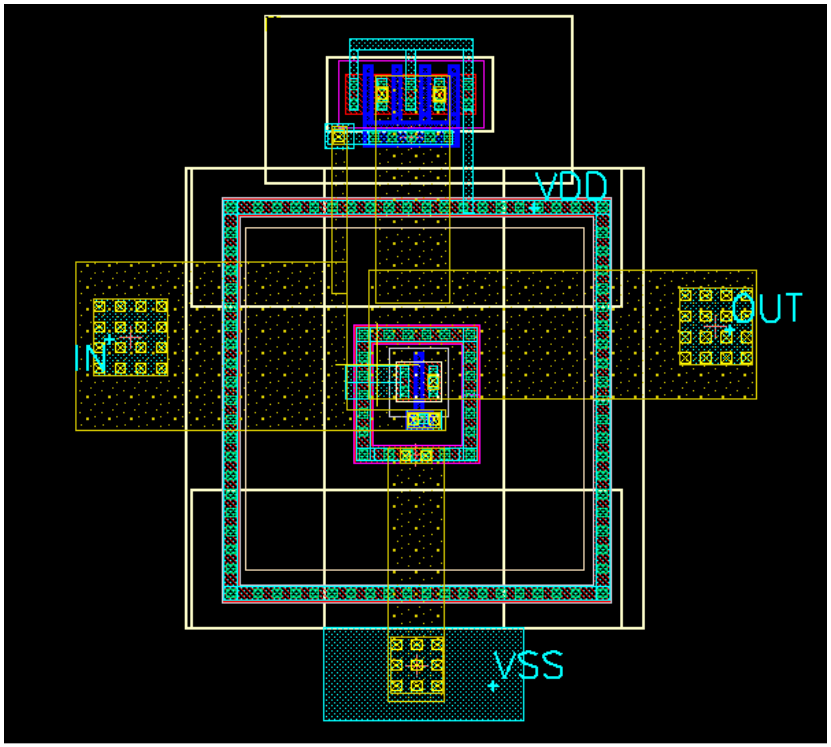
Layout Tool–Laker

- PEX(Parasitic Extraction)
- Parasitic Extraction is calculation of the parasitic effects in both the designed devices and the required wiring interconnects of an electronic circuit.



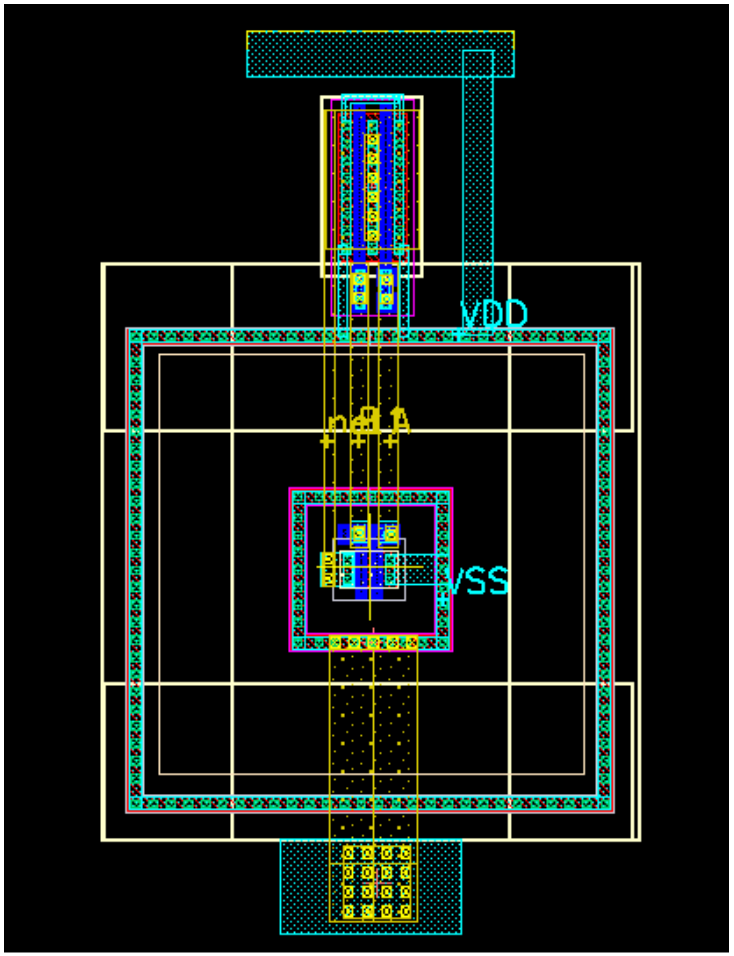


Layout Result – NVERTER




```
.SUBCKT INV IN OUT VDD VSS
xM1 OUT IN VSS VSS nch_mis W=.5u
L=.18u m=1
xM2 OUT IN VDD VDD pch_mis W=.5u
L=.18u m=4
.ends
```

Layout Result – NAND




```
.SUBCKT NAND A B net1  VDD VSS
xM1 net1 A VDD VDD pch_mis W=1u
L=.18u m=4
xM2 net1 A net2 net2 nch_mis W=1u L=.18u
m=1
xM3 net2 B VSS VSS nch_mis W=1u L=.18u
m=1
xM4 net1 B VDD VDD pch_mis W=1u
L=.18u m=4
.ends
```