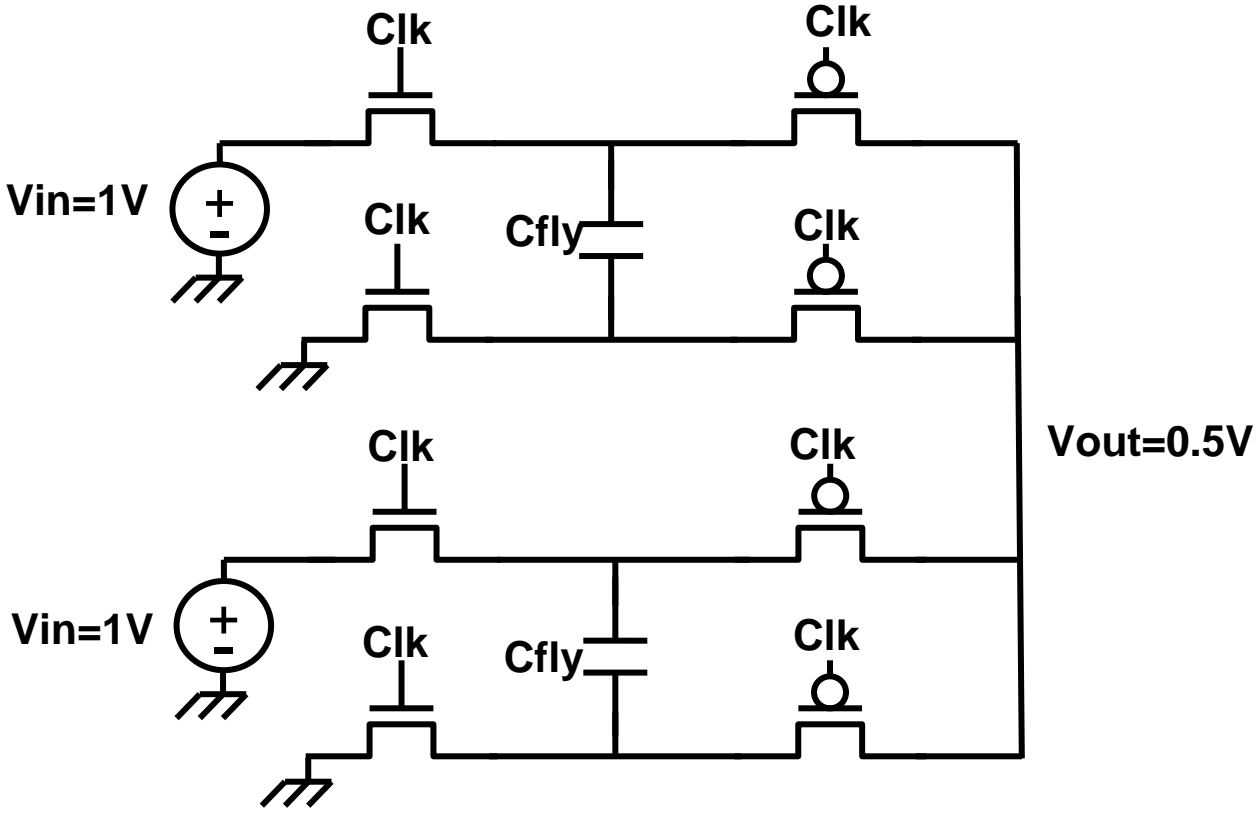


Design Fully Integrated Switched Capacitor

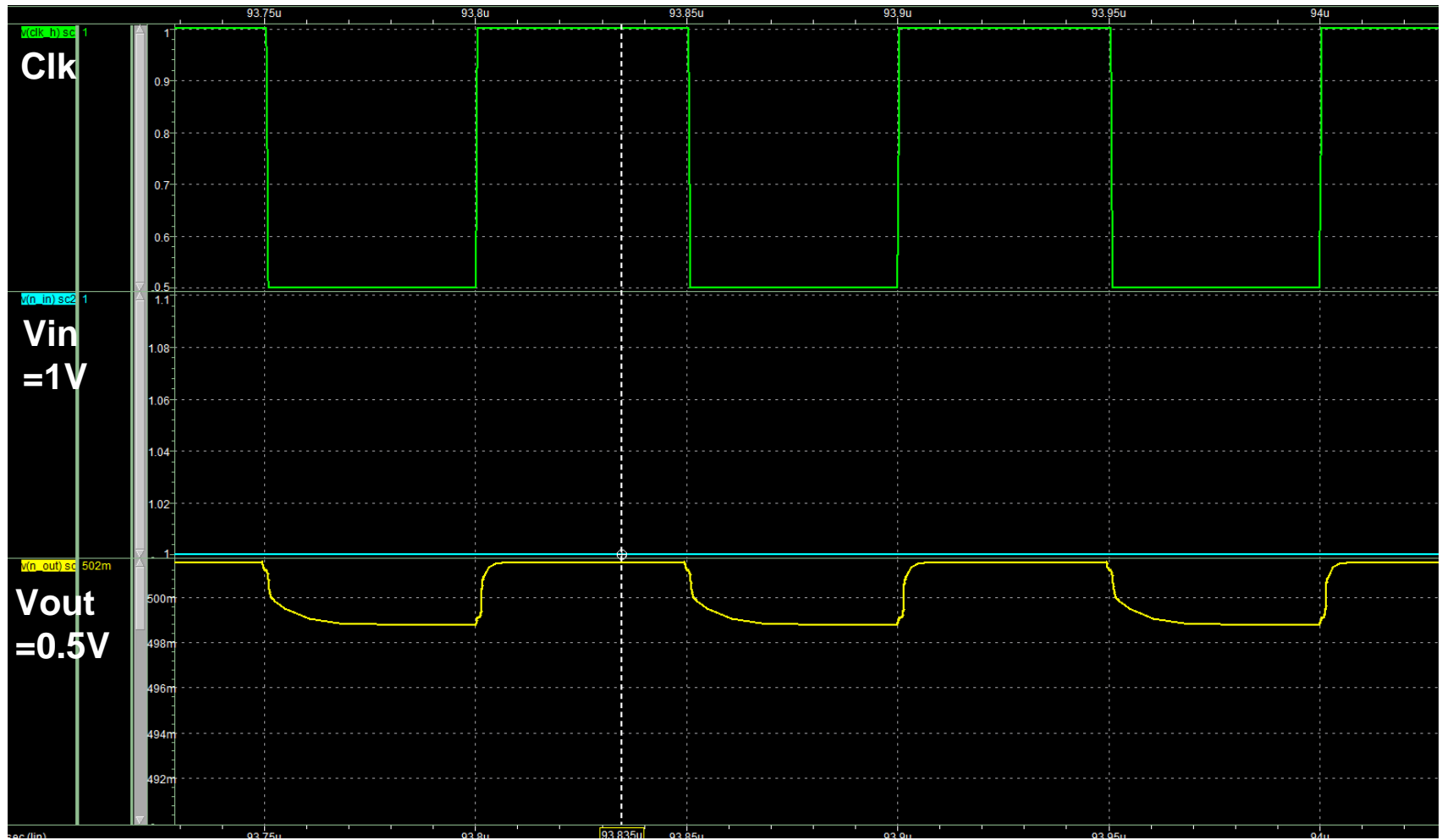
鑽石計畫維基夥伴獎學金

電工系 吳季儒

Switched Capacitor 2:1 Topology



Switched Capacitor Simulation



Simulation Result

- Convert $V_{in}=1V$ to $V_{out}=0.5V$
- Ripple= 4.5mV
- Cfly capacitor= 100fF
- Frequency= 10Mhz
- Efficiency= 81.2%



未來展望

- Add non-overlapping
- Add level shift, to reduce Switching loss
- Complete 3:1 & 3:2 topology
- Higher performance

