Design Fully Integrated Switched Capacitor
Switched Capacitor 2:1 Topology

Vin=1V

Vout=0.5V

Clk

Cfly
Switched Capacitor Simulation

- **Input (Vin)**: 1V
- **Output (Vout)**: 0.5V
Simulation Result

- Convert $V_{in} = 1\text{V}$ to $V_{out} = 0.5\text{V}$
- Ripple = 4.5mV
- $C_{fly}$ capacitor = 100fF
- Frequency = 10Mhz
- Efficiency = 81.2\%
未來展望

- Add non-overlapping
- Add level shift, to reduce Switching loss
- Complete 3:1 & 3:2 topology
- Higher performance